

## Thermal oxidation improvement in semiconductor wafer fabrication

Christopher Julian Mahandran, Abdul Yasser Abd Fatah, Nurul Aini Bani, Hazilah Mad Kaidi, Mohd Nabil Bin Muhtazaruddin, Mohd Effendi Amran

Department of Engineering, Razak Faculty of Technology and Informatics, Universiti Teknologi Malaysia, Malaysia

---

### Article Info

#### Article history:

Received Aug 16, 2018

Revised Jan 12, 2019

Accepted Mar 3, 2019

---

#### Keywords:

Design of experiments

Silicon wafer

Thermal oxidation

Wafer fabrication

---

### ABSTRACT

Thermal oxidation is a process done to grow a layer of oxide on the surface of a silicon wafer at elevated temperatures to form silicon dioxide. Usually, it encounters instability in oxide growth and results in variation in the oxide thickness formed. This leads to downtime of furnace and wafer scrap. This study focuses on the factors leading to this phenomenon and finding the optimum settings of these factors. The factors that cause instability to oxide thickness were narrowed down to location of wafer in furnace, oxidation time, gas flow rate and temperature. Characterization and optimization were done using Design of Experiments. Full factorial design was implemented using 4 factors and 2 levels, resulting in 16 runs. Data analysis was done using Multiple Regression Analysis in JMP software. Actual versus predicted plot is examined to determine whether the model fit is significant. Adjusted  $R^2$  value was obtained at 99.8% or 0.998 indicating that there is very minimal variation of the data not explained by the model and thus confirming that the model is good. From the effect test, the factors were narrowed down from 4 factors to 3 factors. Location factor was found to have no impact. Significant factors that have impact are gas flow rate, oxidation time and temperature. Analyzing the leverage plots and least square mean plots, temperature was found to have the highest impact on oxide thickness. The model was further analyzed using prediction profiler in JMP to find the optimum settings for thermal oxidation process to meet the target oxide thickness of 8000Å. Optimum setting for temperature was found to be at 958 C, gas flow rate at low flow rate (H<sub>2</sub>:6.5 slm and O<sub>2</sub>:4.5 slm), oxidation time at 280 min and location of wafers at both zone 1 and zone 2.

Copyright © 2019 Institute of Advanced Engineering and Science.  
All rights reserved.

---

### Corresponding Author:

Abdul Yasser Abd Fatah,  
Razak Faculty of Technology and Informatics,  
Universiti Teknologi Malaysia,  
Jalan Sultan Yahya Petra, 54100 Kuala Lumpur, Malaysia.  
Email: yasser.kl@utm.my

---

## 1. INTRODUCTION

Semiconductor chips or integrated circuits (IC) are extremely miniaturized chips containing multiple components embedded within [1-6]. Semiconductor manufacturing process starts with raw wafer, predominantly made using silicon wafers [1, 6-9]. These silicon wafers are processed in the wafer fabrication line through the process of oxidation, photolithography, etch, diffusion, deposition, ion implantation and planarization [2, 6-15]. Figure 1 shows the general semiconductor wafer fabrication process flow [16]. After wafer fabrication process, the wafers are sent for probe test to check the electrical distributions and yield, prior to sending to assembly and final test [7, 10-13, 17-20].

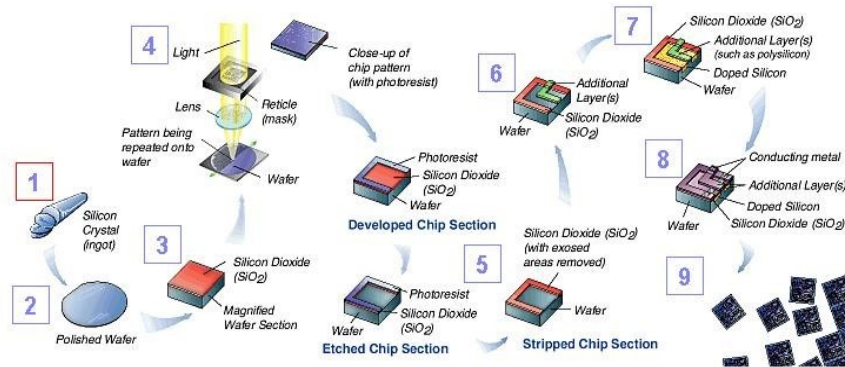
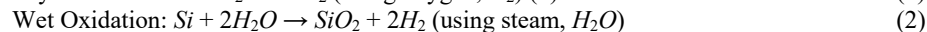
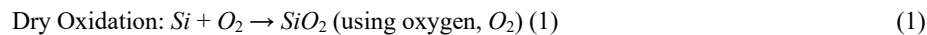


Figure 1. Semiconductor wafer fabrication process flow

One of the critical process in semiconductor wafer fabrication is the thermal oxidation process [6, 8, 9, 11, 12]. Thermal oxidation is a process done to grow a layer of oxide on the surface of a wafer. Thermal oxidation layer acts as a passivation and masking layer for silicon devices. This process is done using oxidation furnaces at elevated temperatures between 600°C to 1250°C to form silicon dioxide layer [6, 7, 13, 21]. There are 2 methods of oxidation, dry and wet oxidation, and they are represented in (1) and (2) [6].



In semiconductor wafer fabrication, thermal oxidation process is done in oxidation furnaces. This oxidation furnace is an integral part of wafer fabrication in the semiconductor industry [2, 6, 8, 11, 12, 21]. It is a thermal processing equipment that process semiconductor wafers at elevated temperatures to perform the oxidation process. Usually, thermal oxidation process encounters instability in oxide growth. This results in variation in the oxide thickness formed. Two main impacts of oxide thickness instability are downtime and scrap. As thermal oxidation has long processing time, any impact on the tool can cause a line down issue which leads to downtime. This will affect the cycle time and on-time-delivery of products. The commitment of product delivery on time is vital in any industry [12].

Maintaining the tool uptime has always been a test in the semiconductor manufacturing industry as industry gets more competitive by the day [17, 20, 22-25]. Tool uptime is an important element towards the manufacturing production output [22]. The tool should be reliable to cope with the production output rate. Another impact is product scrap due to instability in oxide thickness. Scrap happens when the oxide thickness is out of the specification limits. This risk is scrapping a lot of wafers; an observation made in a wafer fabrication company shows that a single run can process up to 288 wafers, which could result in a lot of wafers being wasted.

It is critical for a semiconductor plant to be productive and efficient. The plant needs to reduce or eliminate all factors that disrupt its output performance. One of the main focuses is to reduce downtime of critical tools and improve the tools availability [17, 23]. This is a very complex area as downtime reduction of critical tools needs intense study that anything done does not affect the after product. Equipment downtime is inevitable in a wafer fabrication plant and a single machine down could affect the downstream production process [26]. In general, equipment downtime due to thermal oxidation furnaces are long because once the troubleshooting is done, the tool needs to be tested and each test run is long due to long oxidation process times.

In the operation of thermal oxidation furnaces, multiple input variables are present i.e. temperature, gas, pressure, process duration and zonal location of the furnace. These input variables can have control issues that can affect the performance of the furnace. One dominant problem in the thermal oxidation process is the instability in the thermal oxidation process which causes variation in oxide thickness. This leads to downtime of furnaces and wafer scrap [22, 1]. This study focuses on identifying the factors in thermal oxidation process that affect the variation of oxide thickness. Then, these factors are being analyzed and characterized by using design of experiment (DOE) following the study made by You et al in 2006, albeit on different process and software used [11]. The results will then be used to develop process optimization of the thermal oxidation process.

## 2. RESEARCH METHOD

In order to identify possible factors that affects the variation of oxide thickness, a cause and effect (Ishikawa diagram) was developed. This is done by brainstorming sessions with the team members (Figure 2). Through the diagram, every single possible root cause is listed out. This helps to cover all possibilities before the scope is narrowed down into a specific area. The factors identified to be contributing to instability in the thermal oxidation process was further studied using statistical analysis tools to find out the source of variation. This is done by adopting design of experiments (DOE), where it is shown in Figure 3, the left part of the figure shows design planning and left part shows the full factorial design for 4 factor (Figure 3). Table 1 shows the 4 factors with 2 levels being implemented for DOE purpose.

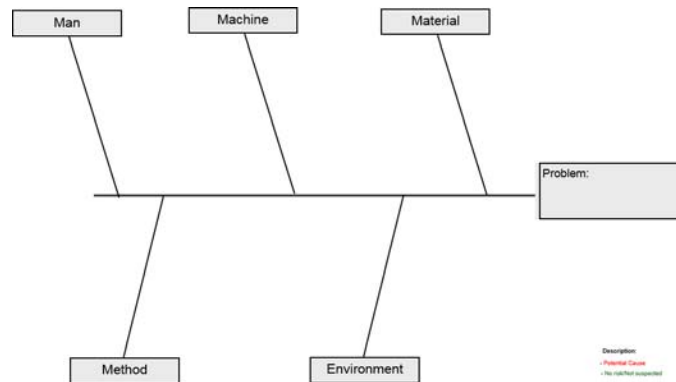


Figure 2. Ishikawa diagram

Table 1. DOE factors with low and high levels

Factors	Levels	
	Low	High
Temperature (°C)	920	980
Gas Flow in Ratio of $H_2:O_2$ , (standard liter per minute, slm)	6.5:4.5	7.5:5.0
Oxidation Time (min)	260	300
Location in Furnace	Zone 1	Zone 2

The experiment was developed based on DOE method. This method was used to analyze the effects of individual variables and to find the optimum combination of values for the process variables in order to improve the process. The experimental design for the DOE of this project was done using a full factorial design with 4 factors and 2 levels, in which  $2^4$  or 16 combinations are required resulting in 16 runs. The experimental design matrix was generated by using JMP (Figure 3) [1, 27].

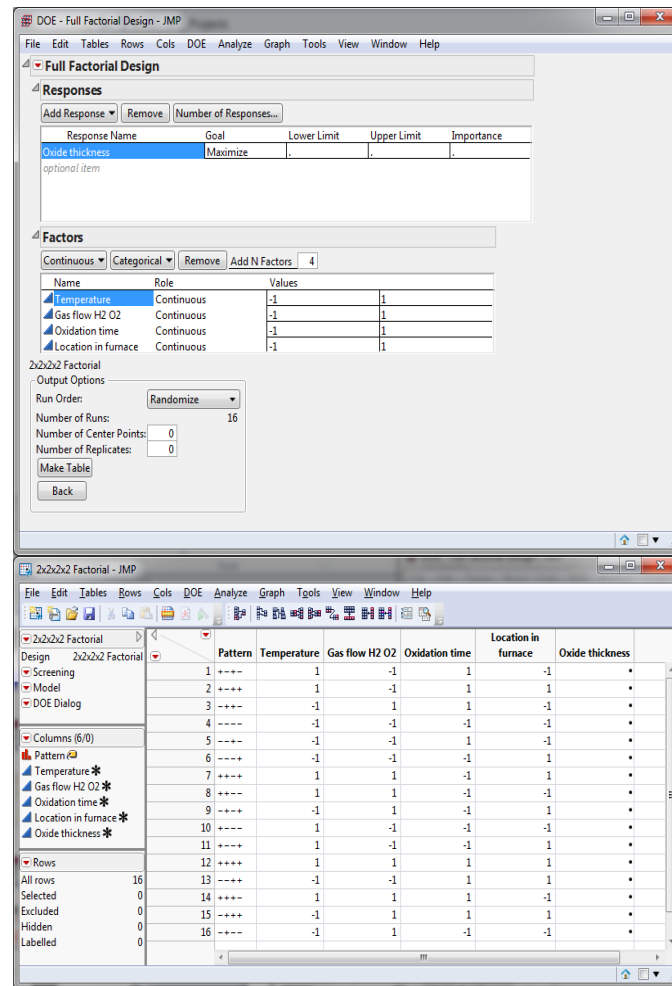


Figure 3. DOE full factorial design planning using JMP (left), the 4 factors design (right)

### 3. RESULTS AND ANALYSIS

In this section, the results of research are shown and discussed. There are three different sub-sections for results in determining the factors that affecting the oxidation of the wafer. These sub-sections are the factors that affecting the process, the result of DOE and the optimum settings as found from the DOE study.

#### 3.1. Factors affecting the process

Through the Ishikawa diagram (Figure 4), every single possible root cause under categories Man, Machine, Material, Method and Environment were listed out so that any possibilities are not missed out. This is helpful to cover all possibilities before the scope is narrowed down into a specific area. Based on the Ishikawa diagram, the factors identified to have contribution on the process was found to be from the machine category, consisting of furnace temperature, gas flows, oxidation time and location of wafers in the furnace [6].

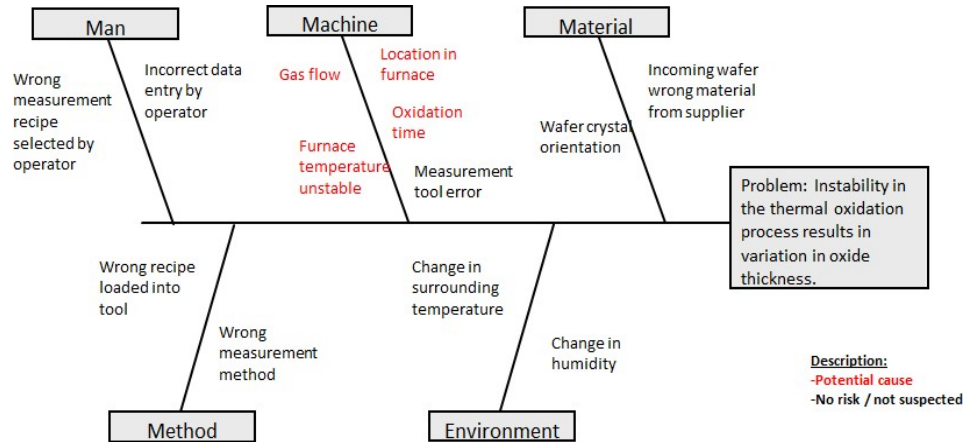


Figure 4. Ishikawa diagram for potential causes of thermal oxidation thickness instability

### 3.2. Results of DOE

Once the factors that affecting the performance of the process had been determined, the experiment will then be carried out according to the run order whereby the 16 runs were randomly arranged. For each run, the variables are varied according to the table and the corresponding oxide thickness on the test wafer is then measured. The data for the DOE is shown in Table 2.

Table 2. DOE data for  $2^4 = 16$  runs

Run	Temp	Gas	Ox Time (mins)	Location	(angstrom, A)					Avg Thick	Range	Std Dev
1	980	Low	300	Zone 1	9527	9613	9432	9444	9642	9532	210	95.4
2	980	Low	300	Zone 2	9629	9525	9401	9624	9538	9543	228	92.8
3	920	Hi	300	Zone 1	6712	6592	6610	6517	6409	6568	303	112.9
4	920	Low	260	Zone 1	5865	5720	5666	5811	5711	5755	199	81.1
5	920	Low	300	Zone 1	6414	6300	6317	6298	6210	6308	204	72.6
6	920	Low	260	Zone 2	5747	5822	5917	5738	5922	5829	184	88.7
7	980	Hi	260	Zone 2	9116	9189	9037	9201	9024	9113	177	82.5
8	980	Hi	260	Zone 1	9044	9121	9218	9017	8888	9058	330	122.8
9	920	Hi	260	Zone 2	6021	5977	6149	6221	5930	6060	291	121.6
10	980	Low	260	Zone 1	8780	8921	8817	8700	8699	8783	222	92.4
11	980	Low	260	Zone 2	8822	8900	8798	8901	8807	8846	103	50.8
12	980	Hi	300	Zone 2	9812	9745	9903	9875	9888	9845	158	65.6
13	920	Low	300	Zone 2	6377	6410	6504	6226	6301	6364	278	105.9
14	980	Hi	300	Zone 1	9911	9774	9837	9710	9801	9807	201	74.6
15	920	Hi	300	Zone 2	6690	6521	6480	6555	6583	6566	210	79.4
16	920	Hi	260	Zone 1	5999	6057	6101	6044	6166	6073	167	63.3

After the data collection from DOE is done, the model is constructed from the data of the DOE, the suitability of the multiple regression model as a whole was checked by referring to the summary of fit section (Figure 5). The coefficient of determination (Rsquare Adj or  $R^2$  adj) was inspected to check if the model is good in terms of prediction ability.  $R^2$  adj always lies between 0 and 1. The closer  $R^2$  adj is to 1, the prediction is more accurate.

Actual versus predicted plot is examined to determine whether the model fit is significant.  $R^2$  adj value is obtained at 99.8% or 0.998. This indicates that 99.8% of Y is predicted by the Xs. This tells us that there is very minimal variation of the data not explained by the model, confirming that this model is good. From the Effect Test, the effect of Location is found not to be significant, since p-value is more than 0.05. Hence, only gas flow, temperature and oxidation time factors are found to have effect on the oxide thickness

### 3.3. Optimum Setting

The target of oxidation thickness for this particular process is 8000A. To achieve this, a function called the Prediction profiler in JMP was used (Figure 6). To optimize the combination of the factors, in the Prediction Profiler function, Optimization and Desirability is selected, followed by Desirability Functions

and then set to Maximize Desirability. The prediction profiler function will then find the optimum factor settings to meet Y (the oxide thickness target).

From the prediction profiler, the optimum settings to meet the target oxide thickness of 8000 Å for temperature is about 958°C. As for the gas flow, only lower H and O gas flow (H: 6.5 slm and O: 4.5 slm) are required. This saves the usage of gas and helps with cost savings indirectly. Oxidation time required is at 280 min. Location has no impact, and therefore both Zone 1 and Zone 2 can be utilized to render the same results (Figure 7).

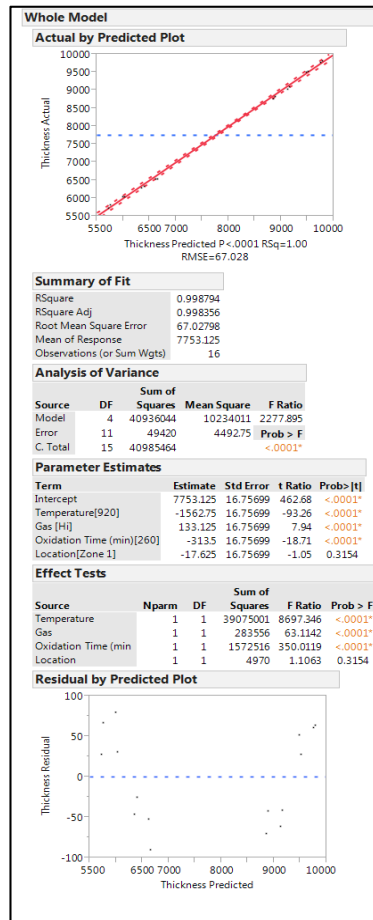


Figure 5. Multiple regression analysis fit model

#### 4. CONCLUSION

The characterization and optimization were done by using Design of Experiments as modified from the study of You et al, 2006 [11]. From the design of experiment, it is shown that the factors that have impact on oxide thickness were identified and are further narrowed down from 4 factors (temperature of furnace, oxidation time, location in the furnace and gas flow rate) into 3 factors only, where the location factor was found to have no impact. Significant factors that have impact on the process are gas flow rate, oxidation time and temperature. Out of the three factors, temperature was found to have the highest impact on oxide thickness process.

#### ACKNOWLEDGEMENTS

The authors would like to express their appreciations and gratitudes towards the Universiti Teknologi Malaysia and Malaysian Ministry of Education for funding this study via grants R.K130000.7740.4J315 and Q.K130000.2540.16H95

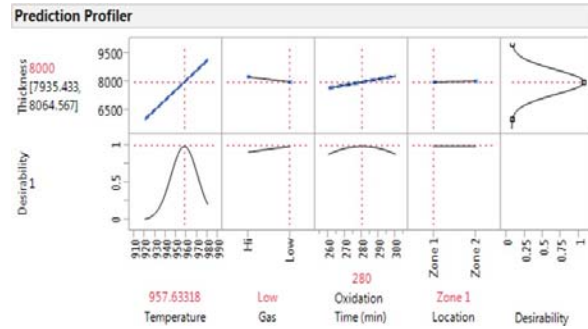


Figure 6. Prediction profiler plot for optimum process settings



Figure 7. Optimum process settings for thermal oxidation

## REFERENCES

- [1] M. A. Chik, K. Ibrahim, M. H. Saidin, F. M. Yusof, G. Devandran, and U. Hashim, "Development of capacity indices for semiconductor fabrication," *2012 10th IEEE International Conference on Semiconductor Electronics, ICSE 2012 - Proceedings*, pp. 649–653, 2012.
- [2] L. Ye, M. P. de Jong, T. Kudernac, W. G. van der Wiel, and J. Huskens, "Doping of semiconductors by molecular monolayers: monolayer formation, dopant diffusion and applications," *Materials Science in Semiconductor Processing*, vol. 57, no. October 2016, pp. 166–172, 2017.
- [3] G. Banky and K. Wong, "Troubleshooting exercises using circuit simulator software: support for deep learning in the study of electronic circuits," *International Conference on Engineering Education*, 2007.
- [4] T. Ogunfunmi and M. Rahman, "A concept inventory for an electric circuits course: Rationale and fundamental topics," *ISCAS 2010 - 2010 IEEE International Symposium on Circuits and Systems: Nano-Bio Circuit Fabrics and Systems*, pp. 2804–2807, 2010.
- [5] A. R. Streveler, M. Geist, R. R. Ammerman, C. Sulzbach, R. Miller, B. Olds, M. Nelson, R. Streveler, M. Geist, and R. R. Ammerman, "Identifying and Investigating Difficult Concepts in Engineering Mechanics and Electric Circuits," *Proceedings of the 2006 American Society for Engineering Education Conference*, p. 227558, 2006.
- [6] C. Barker, A. Badowski, B. Whitefield, K. L. Levien, and M. D. Korestky, "Factors affecting thickness variation of SiO<sub>2</sub> thin films grown by wet oxidation," *IEEE Transactions on Semiconductor Manufacturing*, vol. 24, no. 2, pp. 348–357, 2011.
- [7] N. Wilke, A. Mulcahy, S. R. Ye, and A. Morrissey, "Process optimization and characterization of silicon microneedles fabricated by wet etch technology," *Microelectronics Journal*, vol. 36, no. 7, pp. 650–656, 2005.
- [8] C. Li, Y. Zhang, and H. Dai, "Design and implementation of the control system to vacuum diffusion furnace," *Proceedings of the 32nd Chinese Control Conference*, pp. 6428–6432, 2013.
- [9] J. Ojur Dennis, F. Ahmad, M. Harris Md Khir, and Nor Hisham B Hamid, "Analysis of bonding failure in CMOS MEMS chips," *2013 IEEE Sensors Applications Symposium, SAS 2013 - Proceedings*, pp. 137–141, 2013.
- [10] Y. J. Park and H. R. Hwang, "Minimization of Total Processing Time in Semiconductor Photolithography Process," *Applied Mechanics and Materials*, vol. 325–326, pp. 88–93, 2013.
- [11] H. You, X. Jia, and S. Wang, "The characterization and optimization of the thermal oxidation process equipment using experimental design and data transformation," *2006 25th International Conference on Microelectronics, MIEL 2006 - Proceedings*, pp. 387–390, 2006.
- [12] A. Sonar, S. Shinde, and S. Teh, "Automation: Key to cycle time improvement in semiconductor manufacturing," *ASMC (Advanced Semiconductor Manufacturing Conference) Proceedings*, pp. 93–98, 2013.
- [13] R. P. Chauhan and C. Narula, "Enhanced conduction in CdSe nanowires on 200keV phosphorous negative ion implantation," *Materials Research Bulletin*, vol. 108, no. June, pp. 242–249, 2018.
- [14] S. Lee, J. Won, J. Choi, J. Park, Y. Jee, H. Lee, and D. Byun, "Comparative study on the properties of amorphous carbon layers deposited from 1-hexene and propylene for dry etch hard mask application in semiconductor device manufacturing," *Thin Solid Films*, vol. 519, no. 20, pp. 6683–6687, 2011.
- [15] H. S. Kim, S. K. Eom, K. S. Seo, H. Kim, and H. Y. Cha, "Time-dependent dielectric breakdown of recessed AlGaIn/GaN-on-Si MOS-HFETs with PECVD SiO<sub>2</sub> gate oxide," *Vacuum*, vol. 155, no. June, pp. 428–433, 2018.
- [16] M. D. Guanghua Han, Shuyu Sun, "Capacity Collaboration in Semiconductor Supply Chain with Failure Risk and Long-term Profit," in *Supply Chain Management*, P. Li, Ed. InTech, 2011, ch. 8, pp. 185–200, 2011.
- [17] B. Li, F. Yang, and D. Zhou, "Evidence for self-organized criticality in unscheduled downtime data of equipment," *Journal of Systems Engineering and Electronics*, vol. 25, no. 6, pp. 1020–1026, 2014.
- [18] Y.-C. Chen, R. S. Chen, C. P. Ye, and H. M. Sun, "RFID Application on Manufacturing Process Control in Semiconductor Industry," *Proceedings of the World Congress on Engineering*, vol. 2, pp. 3–5, 2013.
- [19] S. Grubic, J. Restrepo, J. M. Aller, B. Lu, and T. G. Habetler, "A New Concept for Online Surge Testing for the Detection of Winding Insulation Deterioration in Low-Voltage Induction Machines," *IEEE Transactions on Industry Applications*, vol. 47, no. 5, pp. 2051–2058, 2011.
- [20] X. Zhu, "Analysis and improvement of enterprise's equipment effectiveness based on OEE," *2011 International Conference on Electronics, Communications and Control, ICECC 2011 - Proceedings*, pp. 4167–4171, 2011.
- [21] L. M'ouach, J. W. Fowler, S. Dauzère-Péres, S. J. Mason, and O. Rose, "A survey of problems, solution techniques, and future challenges in scheduling semiconductor manufacturing operations," *Journal of Scheduling*, vol. 14, no. 6, pp. 583–599, 2011.
- [22] M. Czerniak, A. Ifould, M. Mooney, and A. Maiorana, "Maintenance pooling to maximize fab uptime," *ASMC (Advanced Semiconductor Manufacturing Conference) Proceedings*, pp. 216–220, 2012.
- [23] C. P. Ahire and A. S. Relkar, "Correlating failure mode effect analysis (FMEA) & overall equipment effectiveness (OEE)," *Procedia Engineering*, vol. 38, pp. 3482–3486, 2012.
- [24] W. Yang and R. Court, "Experimental study on the optimum time for conducting bearing maintenance," *Measurement: Journal of the International Measurement Confederation*, vol. 46, no. 8, pp. 2781–2791, 2013.
- [25] S. Shawn Lee, C. Shao, T. Hyung Kim, S. Jack Hu, E. Kannatey-Asibu, W. W. Cai, J. Patrick Spicer, and J. A. Abell, "Characterization of Ultrasonic Metal Welding by Correlating Online Sensor Signals With Weld Attributes," *Journal of Manufacturing Science and Engineering*, vol. 136, no. 5, p. 051019, 2014.
- [26] Y.-M. Tu and C.-L. Chen, "Model to determine the capacity of wafer fabrications for batch-serial processes with time constraints," *International Journal of Production Research*, vol. 49, no. 10, pp. 2907–2923, may 2011.
- [27] M. Fu, M. Perlman, Q. Lu, and C. Varga, "Pharmaceutical solid-state kinetic stability investigation by using moisture-modified Arrhenius equation and JMP statistical software," *Journal of Pharmaceutical and Biomedical Analysis*, vol. 107, pp. 370–377, 2015.